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# A Hybrid Modular DC Solid State Transformer Combining High Efficiency and Control Flexibility

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***Abstract*- This paper presents a hybrid modular dc solid state transformer (HMDCSST) composed of a series resonant-dual active bridge (SR-DAB) and a phase shift-dual active bridge (PS-DAB), aiming at improving the transfer efficiency as well as maintaining the control flexibility. The key problems in terms of modeling and control strategy are discussed in the paper. The generalized average and small signal models of the HMDCSST are derived and confirmed by simulation, in which two LC filters are also considered to reduce the ripple components of the input and output currents. Based on the models, the control strategies to achieve flexible control of the output voltage and power are designed. Moreover, as a key problem for HMDCSST, the design principle of the number for each type of DAB is discussed to meet the demands of the grid. Finally, a three-module prototype of HMDCSST consisting of one PS-DAB and two SR-DAB modules was built-up and tested, and the results proved that HMDCSST has higher efficiency than the traditional DCSST based on PS-DABs purely, without sacrificing the output voltage and power regulating capability in the meanwhile.**

***Index Terms*- Hybrid modular dc solid state transformer, phase shift-dual active bridge, series resonant-dual active bridge, small signal modelling, control strategy.**

## I. Introduction

In recent years, with the increasing penetration of distributed energy resources and popularization of dc loads such as electric vehicles, the huge potential of dc distribution systems has been recognized, which has great advantages over traditional ac systems in terms of power quality, stability and transmission capacity [1]-[3]. As the key equipment interfacing the medium voltage dc transmission (MVDC) grid and the low voltage dc distribution grid (LVDC), the dc solid state transformer (DCSST) is crucial to facilitating the voltage conversion, power transfer and galvanic isolation functions, and has drawn a wide attention [4]-[5].

In view of the advantages of bidirectional power transfer capability, high power density and modular structure, the series resonant-dual active bridge (SR-DAB) and the phase shift-dual active bridge (PS-DAB) DC/DC converters are widely employed as the core circuit of DCSST [6]-[30]. When SR-DAB operates under open loop control with 50% duty cycle and at the complete resonance frequency of the LC tank, it not only has the advantage of simple control but also provides high conversion efficiency due to the zero-voltage switching (ZVS) and zero-current switching (ZCS) characteristics of all switches [6]. In addition, the voltage transfer ratio of SR-DAB is independent of the loads and switching frequencies, so the voltage gain of the converter is a constant [7], [8]. With advantages above, SR-DAB with the input-series output-parallel (ISOP) structure becomes an ideal solution to construct DCSST. However, with flexible regulation demands of the output voltage, the variable frequency control or phase shift control must be applied. As a consequence, not only the control complexity increases, but also the conversion efficiency decreases due to the lack of ZVS and ZCS [9]-[11]. To keep ZVS working at a light load, the pulse width modulation (PWM) combined with phase shift modulation (PSM) method was addressed in [12]. In order to further widen the soft switching range, the modified dual bridge series resonant converter topology [13], controlled inductor type SR-DAB converter [14] and CLTC type resonant converter with auxiliary transformer [15] based on conventional SR-DAB, were proposed respectively. The overall ZVS can be obtained with above methods. However, these additional switches and components can also increase power losses. To conquer these drawbacks, a four-degree freedom modulation strategy for SR-DAB was proposed in [16]. The overall soft switching range was realized, but the control strategy is too complicated to analyze the system stable region and the reliability cannot be ensured.

As for the PS-DAB converter with single phase shift (SPS) modulation, it can regulate the transfer power and output voltage flexibly by controlling the phase shift ratio between the primary and secondary side bridges, which has been extensively studied and applied to various solid-state transformers. However, it fails to run on ZVS in some situations, such as light load and non-unity voltage gain [17]-[19]. Moreover, under the heavy load and non-unity voltage gain conditions, the circulating current will bring excessive current stress [20]. The potential loss of ZVS and the circulating current will reduce the efficiency of the converter significantly. Some researches provide alternatives of the multiple phase shift control [18], [21]-[22] or the extended phase shift control [23]-[24] to extend the ZVS range. The PS-DAB with conventional dual phase shift exhibits large current and losses if there is a small change of outer phase shift ratio,

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which is caused by the change of command to adjust power transmission. To solve this problem, a novel inner phase shift control with low surge currents and stable power control was proposed in [25]. In [26], a unified triple phase shift control was addressed to achieve ZVS. By decreasing the magnetic inductance and making the design optimization, ZVS region can be extended in [27]. To minimize the circulating current, a three-voltage-level phase shift modulation was presented in [28]. Except for the optimal control method mentioned above, some methods implemented by hardware were proposed in [29] and [30]. In [29], additional active switches in primary and secondary H bridges can restrain the reactive power, but this topology is only suitable for unidirectional power flow. In [30], a hybrid H bridge type DAB converter was presented which can work under full bridge or half bridge mode to maintain the unity voltage gain and minimum reactive power. But these methods are either too complex resulting in a large amount of calculation and a burden of the processor, or they use the additional components which also increase the power losses.

In view of the advantages of the above two kinds of DAB, this paper proposes a new hybrid modular DCSST (HMDCSST) incorporated by SR-DAB and PS-DAB modules. Among the total cells of HMDCSST, the SR-DAB cells transfer the main part of power with high efficiency, while the PS-DABs transfer a small part of power responsible for the output voltage/power regulation. As for its control, the SR-DABs operate under open loop control and at the complete resonance frequency of the LC tank, while the PS-DABs regulate the phase shift ratio through a simple PI controller without any complex calculation. Therefore, the proposed topology can inherit the advantages of the PS-DAB and SR-DAB circuits, i.e. high efficiency, control flexibility and simplicity. What's more, the design complexity is reduced, while the number of the control chips and communication ports is reduced as well, which is conducive to cost saving. The paper takes into account the peak value and ripple suppression of the input/output currents of the DCSST by introducing two LC filters, and the key problems in terms of small signal modeling and control strategy with the LC filters are studied in detail.

It is worth mentioning that the ideas based on *hybrid* were presented in [4] and [31]. In [4], the two converters are with the same topology, called full-bridge dc–dc converter, but the different controls are applied to improve the efficiency. The "main" converter, operating with 50% duty cycle open loop control, processes the majority of power with ZCS, and the other one regulates the power flow of the entire system. In [31], the converter consists of one LLC series resonant converter and one PS-DAB which are in parallel with both dc input side and dc output side. Because the output voltage was always clamped by the LLC resonant part stably, a better response of the output voltage is achieved. Both of the converter systems in [4] and [31] are operated under unidirectional power flow. Different from the above two configurations, the proposed HMDCSST in this paper can be used in some special conditions, such as with a high voltage ratio, in bidirectional power and bus voltage regulation.

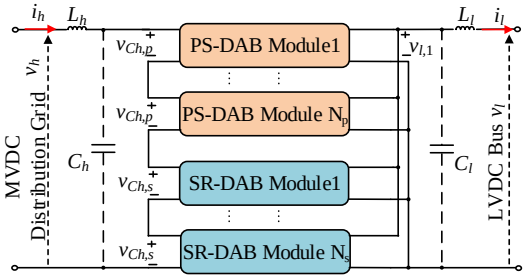


Fig. 1. Simplified configuration of HMDCSST with input/output LC filters.

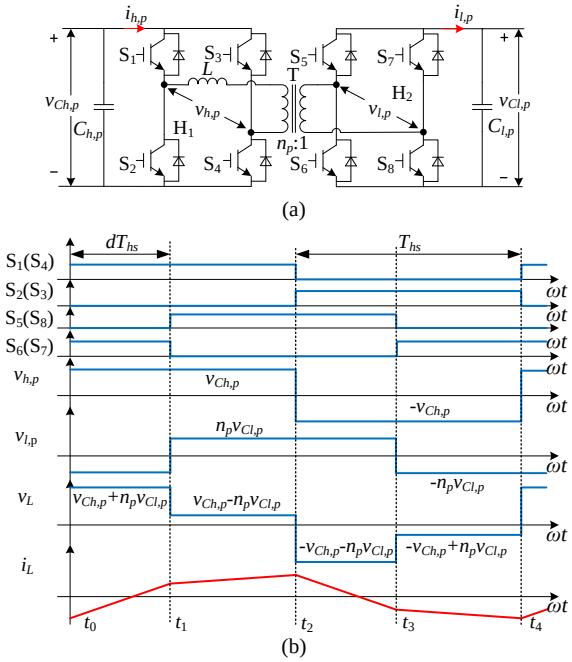


Fig. 2. Topology and SPS control diagram of PS-DAB, (a) topology of PS-DAB and (b) SPS control waveforms.

This paper is organized as follows: In Section II, the large signal average model and small signal model of the HMDCSST considering the input/output LC filters are derived and verified by simulation. The basic operating principle of the HMDCSST is also discussed. Based on the models, the control strategies aiming at achieving flexible control of the output voltage and power with overcurrent suppression are designed in Section III, and the control stability is verified as well. After that, Section IV discusses how to determine the numbers of two-type DAB modules in the HMDCSST. Section V presents the experimental and simulation results, which verifies the good performance of the proposed topology and control. Some issues for improving performance of HMDCSST are discussed in Section VI before this paper is concluded in Section VII.

## II. Modelling of HMDCSST

The simplified configuration of the HMDCSST with input/output LC filters is given in Fig. 1. It consists of $N_p$ PS-DAB modules and $N_s$ SR-DAB modules, which are in series with the dc input side and in parallel with the dc output side, in such way the high input voltage and large output current can be achieved. $v_h$ and $v_l$ represent the dc voltages of the MVDC distribution grid and the LVDC bus respectively,

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while $L_h$, $C_h$, $L_l$ and $C_l$ are the inductance and capacitance of the input/output LC filters of the HMDCSST.

*A. Average Model of PS-DAB*

The detailed diagram of the PS-DAB cell is depicted in Fig. 2(a). It consists of two full bridge circuits ($H_1$, $H_2$), one high-frequency transformer (HFT), and two filter capacitors ($C_{h,p}$, $C_{l,p}$) on the high-voltage and low-voltage sides, respectively. The HFT provides both galvanic isolation and voltage conversion with the turn ratio of $n_p$:1, and the primary-referred leakage inductance $L$ acts as the interface and energy transfer element. $S_1$~$S_4$ are the switches of bridge $H_1$ while $S_5$~$S_8$ constitute bridge $H_2$. $v_{Ch,p}$ and $v_{Cl,p}$ are the dc voltages of the capacitors ($C_{h,p}$, $C_{l,p}$) on the high-voltage and low-voltage sides, respectively. $v_{h,p}$ and $v_{l,p}$ are the ac square-wave voltages imposed by the bridges $H_1$ and $H_2$. $i_{h,p}$ and $i_{l,p}$ are the dc currents of $H_1$ and $H_2$ without capacitor filtering.

To simplify the control design, the most widely used single phase-shift (SPS) control is considered in this paper for PS-DAB, as shown in Fig. 2(b). $S_1$-$S_8$ are the square-wave gate signals with 50% duty cycle for the corresponding switches in Fig. 2(a). $v_L$ and $i_L$ represent the voltage and current of the leakage inductance respectively. As shown in Fig. 2(b), the primary side bridge leads the secondary side bridge by a phase-shift time, defined as $d{\cdot}T_{hs} = d/(2f_s)$, where $d$, $f_s$ and $T_{hs}$ represent the phase shift ratio, switching frequency, and half-switching period, respectively. Figure 2(b) shows a condition that the power is transferred from the primary side to the secondary side, i.e. $d > 0$; similarly, when $d < 0$, the power will be transmitted from the secondary side to the primary side.

According to [19], the full range bi-directional transmitted power of PS-DAB can be given by

$$p_{t,p} = v_{Cl,p} i_{l,p} = \frac{n_p v_{Ch,p} v_{Cl,p}}{2 f_s L} d(1-|d|) \tag{1}$$

The average dc currents of the input/output sides of PS-DAB in one switching period are derived as follows

$$i_{h,p} = \frac{1}{T_{hs}} \int_0^{T_{hs}} i_L(t)dt = \frac{n_p v_{Cl,p}}{2 f_s L} d(1-|d|) \tag{2}$$

$$i_{l,p} = \frac{1}{T_{hs}} \int_0^{T_{hs}} i_L(t)dt = \frac{n_p v_{Ch,p}}{2 f_s L} d(1-|d|) \tag{3}$$

According to (1), the transmitted power characteristics curve of the converter is demonstrated in Fig. 3. As shown, the power monotonically increases over the range of $-0.5 \le d \le 0.5$, and reaches its minimum and maximum value at $d = -0.5$ and $d = 0.5$ respectively, thus the region $\{d \in \mathrm{R} \mid -0.5 \le d \le 0.5\}$ is selected as the effective operation and control interval of the PS-DAB.

Taking the input/output capacitors into account, based on the definition of (2) and (3), the equivalent circuit of the PS-DAB average model can be depicted in Fig. 4. $i_{h,p}$ and $i_{l,p}/n_p$ are the controlled current sources depending on $v_{Ch,p}$, $v_{Cl,p}$ and $d$. Then from the analysis, one can see that the PS-DAB is endowed with high control flexibility by the phase shift ratio $d$, and different control requirements, including the regulations for bidirectional power or for input/output dc voltage, can all be met.

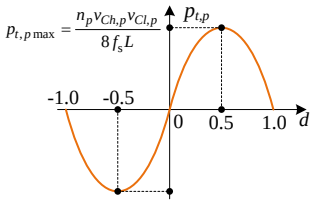


Fig. 3. Transmission power characteristic of PS-DAB.

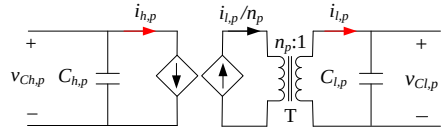


Fig. 4. Equivalent circuit of average model for PS-DAB.

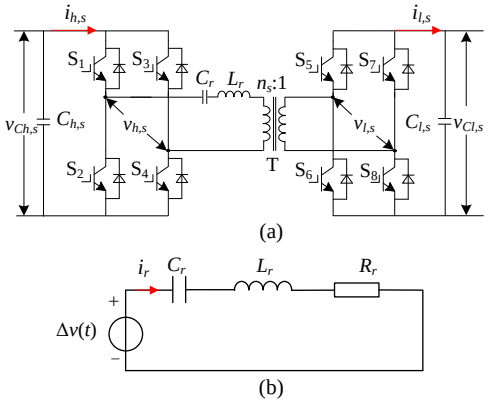


Fig. 5. Topology and alternate equivalent circuit of SR-DAB, (a) topology of SR-DAB and (b) alternate equivalent circuit of SR-DAB.

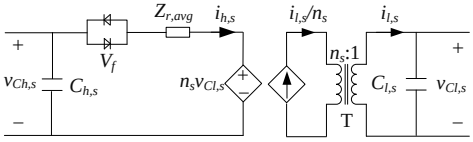


Fig. 6. Equivalent circuit of average model of SR-DAB.

*B. Average Model of SR-DAB*

The SR-DAB converter operates at the full resonance frequency point with open loop control, and all the primary and secondary bridges synchronously work with 50% duty cycle. The frequency $f_s$ is the resonance frequency which equals the switching frequency of PS-DAB in this paper (not necessary, just for convenience). All the series resistances and voltage drop of the switchers in the current path are considered in the modeling of the SR-DAB. For simplicity, the condition with power delivered from the high-voltage side to the low-voltage side is analyzed as an example, and the reverse power condition is similar.

Figure 5(a) shows the circuit diagram of the SR-DAB, with only one series LC resonant tank added compared to the PS-DAB. For clear illustration, the subscript "s" is added to denote the parameters in SR-DAB, including: $C_{h,s}$ and $C_{l,s}$ are the two filter capacitors on both voltage sides of the converter respectively, while $v_{Ch,s}$ and $v_{Cl,s}$ are the average dc capacitor voltages; $v_{h,s}$ and $v_{l,s}$ represent the ac square-wave voltages of the two full-bridges of SR-DAB; and the turn ratio of the HFT is $n_s$:1. In addition, $L_r$ is the resonance inductance in which the

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leakage inductance of the HFT takes as a part, and $C_r$ is the resonance capacitor.

Converted onto the primary side, the alternate equivalent circuit of SR-DAB is exhibited in Fig. 5(b), where $R_r$ is the sum of the circuit equivalent resistances, and $\Delta v(t)$ represents the voltage difference of the square-wave voltages between the primary side and secondary side, as shown in the following equation

$$\Delta v(t)=\begin{cases}+\Delta V, & S_1(S_5),\ S_4(S_8)\ \text{On}\\ -\Delta V, & S_2(S_6),\ S_3(S_7)\ \text{On}\end{cases} \tag{4}$$

where

$$\Delta V = V_{Ch,s} - V_{h,f} - n_s\left(V_{Cl,s}+V_{l,f}\right) \tag{5}$$

Therefore, $\Delta v(t)$ is also a square-wave voltage with 50% duty cycle and frequency of $f_s$. In (5), the equivalent voltage drops of the H-bridge switches on the primary and secondary side, denoted as $V_{h,f}$ and $V_{l,f}$, are taken into account.

In the series resonant circuit, the fundamental wave analysis method is adopted. The average input current of SR-DAB can be calculated by

$$i_{h,s}=\frac{1}{\pi}\int_0^{\pi}\frac{4\Delta V}{\pi R_r}\sin(\omega_0 t)\mathrm{d}\omega_0 t=\frac{8\Delta V}{\pi^2 R_r} \tag{6}$$

where the resonant angular frequency is defined as follows

$$\omega_0 = 2\pi f_s = 1/\sqrt{L_r C_r} \tag{7}$$

Defining $R_{r,avg}=\pi^2 R_r/8$ and substituting it into (6) yield

$$i_{h,s}=i_{l,s}/n_s=\frac{\Delta V}{R_{r,avg}} \tag{8}$$

By defining $V_f = V_{h,f}+n_s V_{l,f}$ and substituting it into (5) and (8), the average circuit model of SR-DAB is obtained, as shown in Fig. 6, where $Z_{r,avg}$ denotes the equivalent mean impedance and equals $R_{r,avg}$.

### *C. Equivalent Average Model of HMDCSST*

Based on the above average model of the PS-DAB and SR-DAB individually, the equivalent average model of the proposed HMDCSST is developed in this section. For expression simplicity, assume that all the circuit parameters between the same type modules are identical, thus the $N_p$ PS-DAB circuits and the $N_s$ SR-DAB circuits of HMDCSST can be equivalent to one PS-DAB module and one SR-DAB module respectively, as demonstrated in Fig. 7. The input/output capacitors of the DABs can also act as the capacitors of the input/output LC filters, so the $C_h$ and $C_l$ in Fig. 1 will not be considered in Fig.7 to simplify the analysis and design.

Since the practical $N_p$+$N_s$ DAB modules shown in Fig. 1 are connected in series on input side, the input currents $i_{h,p}$ and $i_{h,s}$ of the two equivalent modules in Fig. 7 are the same, as depicted in Fig. 1, satisfying the equation (2) and equation (6) respectively. Similarly, due to the parallel connection, the output voltage in Fig. 7 is the same as that in Fig. 1, denotes as $v_{l,1}$. Other parameters of the equivalent average model, including the input voltages $v_{h1}$ and $v_{h2}$, the turn ratio of the HFTs $n_1$ and $n_2$, and the output currents $i'_{l,p}$ and $i'_{l,s}$, satisfy the following constraints

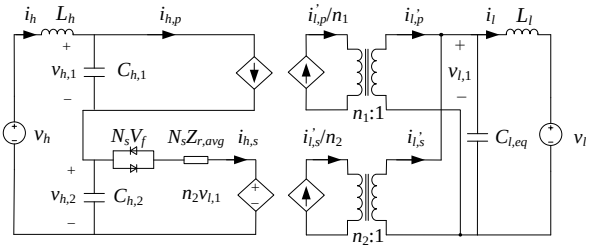


Fig. 7. Equivalent circuit of average model for HMDCSST.

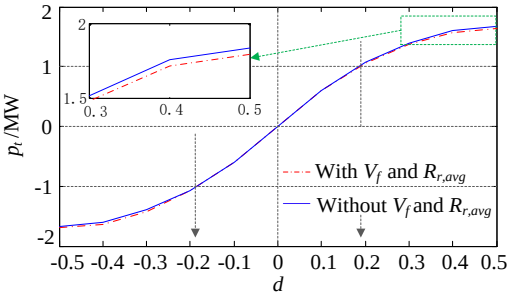


Fig. 8. Power transfer curve of HMDCSST.

$$\begin{cases} v_{h,1}=N_p v_{Ch,p} \\ v_{h,2}=N_s v_{Ch,s} \end{cases} \tag{9}$$

$$\begin{cases} n_1=N_p\cdot n_p \\ n_2=N_s\cdot n_s \end{cases} \tag{10}$$

$$\begin{cases} i'_{l,p}=N_p\dfrac{n_p v_{Ch,p}}{2f_s L}d(1-|d|)=\dfrac{n_p v_{h,1}}{2f_s L}d(1-|d|) \\ i'_{l,s}=N_s i_{l,s}=N_s n_s i_{h,s}=n_2 i_{h,s} \end{cases} \tag{11}$$

The input equivalent capacitors $C_{h1}$, $C_{h2}$, and the output equivalent capacitor $C_{l,eq}$ can be expressed as

$$\begin{cases} C_{h,1}=C_{h,p}\dfrac{1}{N_p} \\ C_{h,2}=C_{h,s}\dfrac{1}{N_s} \\ C_{l,eq}=N_p C_{l,p}+N_s C_{l,s} \end{cases} \tag{12}$$

Then according to the average model stated above, the expressions of the output current and transmitted power of the HMDCSST are described in (13) and (14) respectively. The transfer curve of the power is displayed in Fig. 8 with the parameters listed in Table I.

$$i_l=\frac{d_f\left(v_h-N_sV_f\right)-d_f^2 N_s R_{r,avg} v_l}{1+d_f^2 N_s R_{r,avg} R_l} \tag{13}$$

$$p_t = i_l\cdot v_l \tag{14}$$

where

$$d_f=\frac{n_p d(1-|d|)}{2f_s L}$$

From Fig. 8, one can see that the parameter $V_f$ and $R_{r,avg}$ have little effect on the power transfer characteristics. Let $V_f$

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$=R_{r,avg}=0$ and substitute it in to (13), then the following equation can be obtained

$$i_l = \frac{n_p d(1-|d|)v_h}{2 f_s L} \tag{15}$$

As can be seen from (15), when $V_f$ and $R_{r,avg}$ are neglected, the power transfer characteristic of the proposed HMDCSST is similar as that of the traditional DCSST made up by PS-DAB purely.

### *D. Small Signal Modelling with LC Filters*

Based on the equivalent average model given in subsection C, the small-signal modelling for HMDCSST is developed in this subsection.

Applying small signal perturbations to the variables around the steady-state operating point, that is

$$\begin{cases} v_h = V_h + \hat{v}_h \\ v_l = V_l + \hat{v}_l \\ d = D + \hat{d} \end{cases} \tag{16}$$

$$\begin{cases} i_h = I_h + \hat{i}_h \\ i_{h,p} = I_{h,p} + \hat{i}_{h,p} \\ i_{h,s} = I_{h,s} + \hat{i}_{h,s} \\ v_{h,1} = V_{h,1} + \hat{v}_{h,1} \\ v_{h,2} = V_{h,2} + \hat{v}_{h,2} \end{cases} \tag{17}$$

$$\begin{cases} i'_{l,p} = I'_{l,p} + \hat{i}'_{l,p} \\ i'_{l,s} = I'_{l,s} + \hat{i}'_{l,s} \\ i_l = I_l + \hat{i}_l \\ v_{l,1} = V_{l,1} + \hat{v}_{l,1} \end{cases} \tag{18}$$

where the variables with the superscript "^" are the small signal variations, and the variables capitalized denote the steady-state operating point parameters.

The small signal modelling of HMDCSST takes account of the energy storage process in the SR-DAB, i.e., the equivalent inductance $L_{r,avg}$ is included, with which the equivalent impedance of the SR-DAB is modified as

$$Z_{r,avg}=R_{r,avg}+L_{r,avg} \text{ and } L_{r,avg}=\pi^2 L_r/4 \tag{19}$$

By substituting (16) ~ (19) into the previous equivalent average model circuit, the small signal description of the HMDCSST can be derived, illustrated as follows.

First, the small signal state equations constrained by the entire ISOP system are

$$\begin{cases} C_{h,1}\dfrac{d\hat{v}_{h,1}}{dt} = \hat{i}_h - \hat{i}_{h,p} \\ C_{h,2}\dfrac{d\hat{v}_{h,2}}{dt} = \hat{i}_h - \hat{i}_{h,s} \\ C_{l,eq}\dfrac{d\hat{v}_{l,1}}{dt} = \hat{i}'_{l,p} + \hat{i}'_{l,s} - \hat{i}_l \end{cases} \tag{20}$$

$$\begin{cases} L_h\dfrac{d\hat{i}_h}{dt} = \hat{v}_h - \hat{v}_{h,1} - \hat{v}_{h,2} \\ L_l\dfrac{d\hat{i}_l}{dt} = \hat{v}_{l,1} - \hat{v}_l \end{cases} \tag{21}$$

Second, the small signal equations obtained by the module constraint of the PS-DAB module are

$$\begin{cases} \hat{i}_{h,p} = x\hat{d} + y\hat{v}_{l,1} \\ \hat{i}'_{l,p} = z\hat{d} + y\hat{v}_{h,1} \end{cases} \tag{22}$$

And the small signal equations obtained by the constraints of the SR-DAB module are

$$\begin{cases} \hat{v}_{h2} = N_s R_{r,avg}\hat{i}_{h,s} + n_2\hat{v}_{l,1} + N_s L_{r,avg}\dfrac{d\hat{i}_{h,s}}{dt} \\ \hat{i}_{h,s} = \hat{i}'_{l,s}/n_2 \end{cases} \tag{23}$$

where the intermediate variables $x$, $y$ and $z$ are defined as

$$\begin{aligned} x &= n_p\left(1-2|D|\right)V_{l,1}/\left(2 f_s L\right) \\ y &= n_p D\left(1-|D|\right)/\left(2 f_s L\right) \\ z &= n_p\left(1-2|D|\right)V_{h,1}/\left(2 f_s L\right) \end{aligned} \tag{24}$$

The small signal circuit of HMDCSST has the same structure with the average circuit shown in Fig. 7, except that the corresponding variables are represented by small signal ones and are constrained by (20)-(24).

The energy storage components of the circuit can be described in the form of complex frequency domain

$$\begin{cases} Z_h = sL_h \\ Z_l = sL_l \\ Z_{r,avg} = R_{r,avg} + sL_{r,avg} \\ Z_{h,1} = 1/sC_{h,1} \\ Z_{h,2} = 1/sC_{h,2} \\ Z_{l,eq} = 1/sC_{l,eq} \end{cases} \tag{25}$$

Applying the Laplace transformation to (20)-(23), the control-to-output transfer function can be derived as

$$G_1(s) = \frac{\hat{i}_l}{\hat{d}}\Big|_{\hat{v}_h=\hat{v}_l=0} = \frac{A(s)}{B(s)} \tag{26}$$

Here, the intermediate variables $A$(s), $B$(s), $a_1$, $a_2$, $b_1$, $b_2$, and $b_3$ are defined as follows

$$A(s) = (b_1 - a_2)z + (a_2 y - n_2)b_3$$

$$B(s) = \left(Z_l/Z_{l,eq}+1\right)(b_1-a_2) - n_2(a_1-b_2) + y(a_1 b_1 - a_2 b_2)$$

$$a_1 = n_2\left(Z_h + Z_{h,2}\right)Z_l/Z_{h,2}$$

$$a_2 = \left(N_s Z_{r,avg} Z_h + N_s Z_{r,avg} Z_{h,2} + Z_{h,2} Z_h\right)/Z_{h,2}$$

$$b_1 = \frac{Z_{h,1} N_s Z_{r,avg}}{Z_h + Z_{h,1}}, \quad b_2 = \frac{n_2 Z_{h,1} Z_l + y Z_{h,1} Z_l Z_h}{Z_h + Z_{h,1}},$$

$$b_3 = \frac{x Z_{h,1} Z_h}{Z_h + Z_{h,1}}$$

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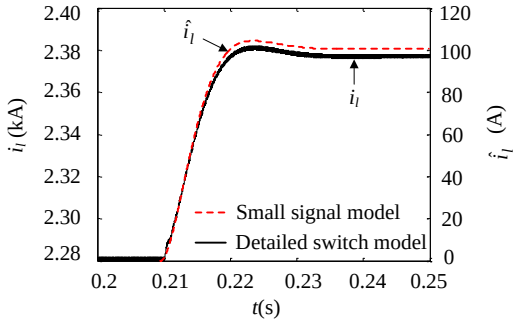


Fig. 9. Comparison of step response of developed small signal model and detailed switching model for HMDCSST.

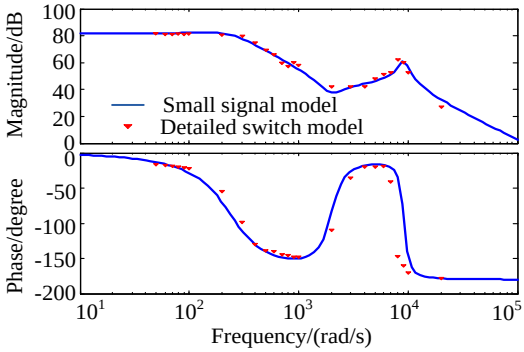


Fig. 10. Bode plot comparison of control-to-output transfer function with $D$=0.18.

### *E. Simulation Verification of Small Signal Model*

In order to verify the accuracy of the developed small signal model, a detailed switching circuit of HMDCSST is developed in MATLAB/Simulink, and result comparisons in both time domain and frequency domain are made.

The simulation model is constructed based on Fig. 1, with three SR-DAB and two PS-DAB modules included. The rated voltages are 10kV and 400V on the high-voltage and low-voltage sides respectively, and the rated power is 1MW. The detailed circuit parameters of HMDCSST are listed in Table I.

Assuming the system starts out at a steady state, with corresponding operating point of $D$=0.18, a step perturbation in the phase shift ratio with $\hat{d}$=0.01 is applied to the above two models. The output current results ( $\hat{i}_l$ ) by the developed model and simulation are depicted in Fig. 9. As demonstrated, the high degree of similarity between the two step responses in the shape confirms the validity of the developed small signal model of HMDCSST.

A comparison of frequency responses between the developed model and the detailed switching model of the HMDCSST is given in Fig. 10. The solid lines represent the calculation results of the developed model, denoted as $G_1$ in equation (26), and the triangles mark the simulation results of the detailed switching model. As can be observed in Fig. 10, there is no significant deviation between the calculated response and simulation ones in the low frequency range. When the frequency (disturbance) is greater than 7,000 rad/s, the deviation becomes obvious and increases with the frequency. This is because the general state-space averaging technique is no longer applicable when the frequency is close to the switching frequency, in other words, in this case the small ac variations cannot be equivalent to dc variations. However, such a comparison in Fig. 10 has proved the effectivity of the proposed small signal model for HMDCSST, which can be used for stability analysis and controller design in Section III.

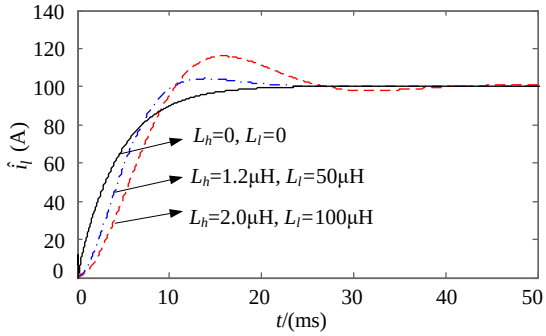


Fig. 11. Comparison of step responses of control-to-output transfer function with different inductance parameters of LC filters.

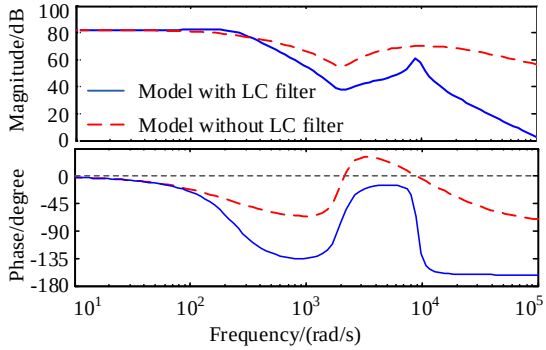


Fig. 12. Frequency responses of control-to-output transfer function based on the developed model with and without LC filters.

Furthermore, to get the effects of the input/output LC filters on the system, comparison results of the step response and frequency domain response with different LC filters are plotted in Fig. 11 and Fig. 12.

In Fig. 11, the step response of the output current $\hat{i}_l$ with $L$ values of the filters being zero is plotted in the solid line, whereas the two dotted lines represent the step currents with different $L$ values. It can be seen that the overshoot of the step current increases with the increase of the inductance. So, from the point of view of dynamic control performance, a smaller series inductance is beneficial to alleviating the overshoot. However, the filter inductances decreasing to zero could deteriorate the power quality of the MV/LV DC grids connected to the HMDCSST, since the high frequency harmonic components of the input/output currents arise. In the light of this, a tradeoff between the power quality and the dynamic characteristics is thereby necessary.

In Fig. 12, the solid line represents the Bode response of the control-to-output transfer function considering the LC filters, while the dotted line represents the curve without considering the LC filters. As can be concluded, the LC filter has a significant inhibitory effect on the high-frequency

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disturbances, and it causes a greater delay in phase which may slow down the system response. Therefore, during the control design and system stability analysis process, the impact of the LC filters must be considered in the modeling to prevent the deviation between theoretical design and actual performance.

## III. Controller Design and Stability Analysis

### A. Controller Design

According to different situations that the HMDCSST is applied, two operating modes, the constant power and the constant voltage, are presented and shown in Fig. 13 and Fig. 14 respectively.

First, in Fig. 13, in the closed-loop feedback control block diagram of the constant power condition, the controlled object is the output power $i_l \cdot v_{l,1}$ behind the filter capacitor $C_{l,eq}$. A PI controller is utilized. For that the voltage of the dc grid at the low-voltage side is constant, the constant power control is actually the constant current control.

To improve the dynamic response, a virtual inner current controller $G_2$ is inserted, which is similar to the conventional dual-loop control but without the high-frequency fluctuation current feedback of the converter, thereby high precision current sensors can be avoided. The current reference $i_l^*$ is the output of the outer power PI controller, and the phase shift ratio $d$ is the output of the virtual current controller $G_2$. The transfer function $G_1$ represents the converter dynamics, as described in (26).

According to (15), the relationship between $i_l^*$ and $d$ is derived, stated as follows

$$i_l^* = i_l = \frac{n_p d(1-|d|)v_h}{2 f_s L} \tag{27}$$

Where $V_f$ and $R_{r,avg}$ are neglected, but the resulting control error and other errors caused by measurement and modeling can all be compensated by the PI controller.

Then applying small signal analysis to (27), the transfer function $G_2$ can be obtained

$$\frac{d}{i_l^*} = G_2 = \frac{2 f_s L}{n_p V_h (1\text{-}2|D|)} \tag{28}$$

It is worth noting that the transfer function (28) is suitable for the bidirectional power flow condition.

Since the capacitance voltage of HMDCSST is 0 at low voltage side before start-up, there will be a very large input deviation of the PI controller during the start-up time, which leads to extremely high accumulated error due to the integrator. It will deteriorate the dynamic characteristics and even threaten the stability of the system.

There are two options to deal with the start-up problems mentioned above: one is adding a limiter (limiter 1 as shown in Fig. 13) to restrict the input deviations of the PI controller, the other is adopting a pre-charge start process in practical operation. Similarly, limiter 2 is responsible for reducing the surge of the output current and therefore alleviating the current stress of the PS-DAB and SR-DAB modules effectively.

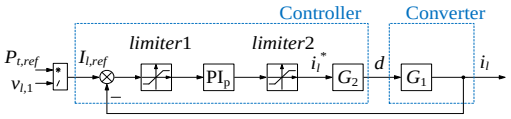


Fig. 13. Control block diagram in constant power scenario.

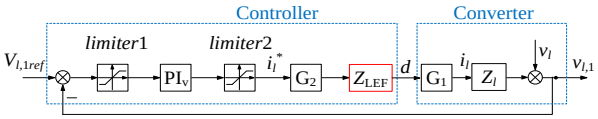


Fig. 14. Control block diagram in constant voltage scenario.

Secondly, when the HMDCSST operates in the constant voltage scenario, the control block diagram is shown in Fig. 14, where $i_l^*$ is the output of the voltage PI controller with a current limiter, and the phase shift ratio $d$ is the output of the current controller $G_2$, obtained by the equation of $d=i_l^* G_2$.

### B. Stability Analysis

From Fig. 13, the open loop transfer function of the output current $i_l$ against its reference $I_{l,ref}$ of the DCSST under constant power condition is obtained

$$G_{c1}=G_{\mathrm{PI_p}} G_1 G_2 \tag{29}$$

According to Fig. 14, the open loop transfer function of the output voltage $v_{l,1}$ against the reference $V_{l,1ref}$ of the HMDCSST under constant voltage control is obtained as in (30).

$$G_{c2}=G_{\mathrm{PI_v}} G_1 G_2 Z_l \tag{30}$$

Then from (29) and (30), the Bode diagrams of the control system under the constant power control and the constant voltage control are plotted in Fig. 15 (a) and (b), respectively, in which the Bode diagrams of their closed loop transfer functions were also given to show the closed loop performances.

It can be seen from Fig. 15(a) that the phase margin is 50.2°, the crossover frequency is 633 rad/s, and the closed loop bandwidth is 850 rad/s under the constant power control, which are the parameters demonstrating stability of the control system. However, in the constant voltage mode as shown in Fig. 15(b), the originally designed phase curve (without LEF) is above 0 degree in the neighborhood of the resonance frequency (about $10^4$ rad/s), which may bring harmonic instability issues. To resolve this problem, a lag element filter (LEF) is plugged into the voltage control loop to reshape the bode response at the critical point in high frequency range. Here the transfer function of the LEF is given by

$$G_{LEF}(s) = \frac{\beta}{1/\omega_f s + 1} \tag{31}$$

where $\omega_f$ determines the phase-lag-compensation frequency band, selected as $\omega_f$ =4000 rad/s according to the original phase curve in Fig. 15(b); $\beta$ determines the magnitude compensation and is set to 1 in this paper, which will not influence the magnitude characteristic of the voltage control loop. Then the transfer function after LEF compensation can be obtained

$$G_{c2}=G_{\mathrm{PI_v}} G_1 G_2 Z_l G_{LEF} \tag{32}$$

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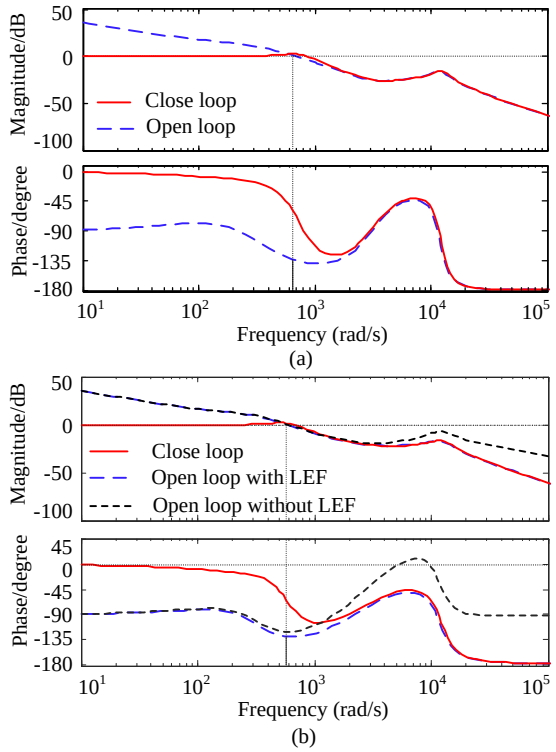


Fig. 15. Bode diagrams of open-loop/closed-loop transfer functions under (a) constant power control and (b) constant voltage control.

The Bode diagrams after the phase lag compensation being plugged in are depicted in blue as shown in Fig. 15(b), where both the magnitude and the phase responses are improved in the high frequency range effectively. The phase margin is 50°, crossover frequency is 588 rad/s, and the closed loop bandwidth is 672 rad/s. Due to the phase change, the phase response deviates away from the zero line and stabilizes the constant voltage control system with sufficient stability margins.

## IV. System Design Consideration

The HMDCSST utilizes two kinds of DAB modules to realize the voltage conversion and power transfer functions and by which the efficiency is also improved. In addition, the control and design are simplified. In this section, a key problem for the proposed HMDCSST is discussed, that is, how to determine the number of each type of DAB.

As can be seen in Fig.1, there are $N_p$ PS-DABs and $N_s$ SR-DABs. In terms of efficiency, the larger number of the SR-DAB modules in the system, the higher efficiency can be achieved. However, there are some limits that constrain the number of SR-DABs in the HMDCSST.

### *A. Input Voltage Unbalance between PS-DAB and SR-DAB*

In the HMDCSST, the SR-DABs always work under fully resonance with the switching frequency equal to the resonant frequency and the duty cycle fixed to 50%, and they do not participate in close-loop control and only transfer power, which is similar to a high efficiency passive transformer. When the load changes or the dc bus voltages deviate from their rated value, the module input voltage distribution changes accordingly.

In the steady state, the voltage relationship between the input voltage of HMDCSST and DABs is

$$v_h = N_p v_{Ch,p} + N_s v_{Ch,s} \tag{33}$$

And the input voltage of SR-DAB can be expressed as

$$v_{Ch,s} = V_f + R_{r,avg} i_{h,s} + n_s v_l \tag{34}$$

The ratio of the single PS-DAB module input voltage to the single SR-DAB module input voltage is used to define the input voltage unbalance factor, as shown below

$$N_v = v_{Ch,s} / v_{Ch,p} \tag{35}$$

By combining (33) and (34), the following expression can be obtained

$$N_v = \frac{V_f + R_{r,avg} i_{h,s} + n_s v_l}{[v_h - N_s (V_f + R_{r,avg} i_{h,s} + n_s v_l)] / N_p} \tag{36}$$

As can be seen from (36), as an inherent characteristic of HMDCSST, the input voltage unbalance between PS-DAB and SR-DAB changes not only with the loads and the bus voltages, but also with the module number and the transformer ratio.

In addition, according to (33) and (34), if $V_f$ and $R_{r,avg}$ are ignored, $v_{Ch,s} \approx n_s v_l$, which indicates that the input voltage of the SR-DAB are clamped to be nearly equal to $n_s$ times of the output voltage, and the input voltage of PS-DAB becomes

$$v_{Ch,p} \approx (v_h - N_s n_s v_l) / N_p \tag{37}$$

When the voltages of MVDC and/or LVDC bus deviate from their rated value, the deviated voltage $\Delta v_{Ch,p}$ is undertaken by all the PS-DABs. The worst case is that $v_h$ reaches its maximum value, while $v_l$ reaches its minimum value simultaneously. In such condition, $\Delta v_{Ch,p}$ must be limited since every DAB module has its block voltage due to the semiconductor devices.

$$\Delta v_{Ch,p} = (\Delta v_h - N_s n_s \Delta v_l) / N_p \le \Delta v_{Ch,p\_\max} \tag{38}$$

Where $\Delta v_{h,p\_\max}$ is the maximum value of $\Delta v_{h,p}$. As can be concluded from (38), a larger $N_p$ is beneficial to satisfying this condition, but it is not good for the work efficiency of HMDCSST.

### *B. Voltage Gain and ZVS Characteristic of PS-DAB*

The voltage gain of the PS-DAB is

$$M = n_p v_l / v_{Ch,p}, \text{if } d \ge 0 \tag{39}$$

$$M = v_{Ch,p} / n_p v_l, \text{if } d < 0 \tag{40}$$

According to (33), (34) and (35),

$$M = \frac{n_p v_l}{V_f + R_{r,avg} i_{h,s} + n_s v_l} N_v, \text{if } d \ge 0 \tag{41}$$

$$M = \frac{V_f + R_{r,avg} i_{h,s} + n_s v_l}{n_p v_l} \frac{1}{N_v}, \text{if } d < 0 \tag{42}$$

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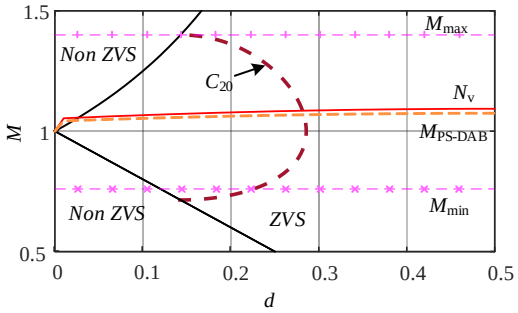


Fig. 16. ZVS curve of PS-DAB with SPS.

As can be seen from equations (41) and (42), if $V_f$ and $R_{r,avg}$ are ignored and the PS-DAB has the same transformer ratio as the SR-DAB, the input voltage unbalance will also make the voltage gain of PS-DAB deviate from its unit gain, and even result in PS-DABs working out of their ZVS zone.

The soft switching conditions of PS-DAB with single phase shift control is determined by $d$ and the voltage gain $M$. It should be pointed out that the condition that the value of $d$ is greater than 0.35 shall be avoided when the reactive current and the power regulating flexibility are considered [19]. However, the smaller values of $d$ will reduce the ranges of ZVS. Moreover, as presented in [33], when $M$>1, the current stress will increase with the increase of $M$; whereas, when $M$<1, the current stress will increase with the decrease of $M$. Therefore, $M$ should also be limited according the operating voltages.

Figure 16 gives a possible range of $d$ and $M$ that can be used to design PS-DAB with all the factors above considered. In the figure, the $N_v$ drawn in red solid line and $M_{PS-DAB}$ drawn in red dash line are given under the rated voltage with $N_p$=1 and $N_s$=4. It can be seen that $N_v$ and $M$ is nearly equivalent when $d \geq 0$, which means the value of $N_v$ close to 1 is beneficial to ZVS. The $C_{20}$ drawn in dashed line is the boundary that the reactive current is less than 20% of the active current.

### *C. Combination of $N_p$ and $N_s$*

For a specific application of HMDCSST, the rated voltages of MVDC/LVDC bus, bus voltage limitations, and rated power are fixed. According to the voltage and power of DAB modules, the total number of PS-DABs and SR-DABs could be determined. For better modular design, the PS-DAB and SR-DAB should employ the same power devices and transformers to reduce the complexity of design and manufacturing, which means the transformer ratio should be the same.

To improve the efficiency while ensuring the operation safety as well, an optimal combination of $N_p$ and $N_s$ can be obtained by following step and an example is taken for illustration. The system parameters are given in Tab. I.

First, the transformer ratio and the total number of HMDCSST can be designed according to the rated voltages of the DAB modules and the rated bus voltages; here $n_p$=$n_s$=5 and $N_{ps}$=$N_p$+$N_s$=5. Moreover, the minimum and maximum values of $M$ are calculated, and in the case, $M_{min}$=0.76 and $M_{max}$=1.4, which nearly equal the limit of $N_v$ according to (41).

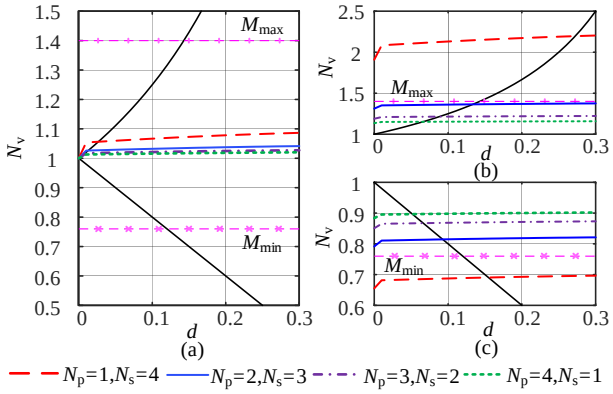


Fig. 17. $N_v$ curve of HMDCSST with different $N_p$ and $N_s$: (a) at the rated values of $V_h$ and $V_l$ , (b) at 1.05$V_h$ and 0.95$V_l$ and (c) at 0.95$V_h$ and 1.05$V_l$.

TABLE I
SIMULATION PARAMETERS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_h$ | 10 kV±5% | $V_{Ch,p}$, $V_{Ch,s}$ | 2 kV±25% |
| $V_l$ | 400 V±5% | $n_p$, $n_s$ | 5 |
| $P_t$ | 1 MW | $N_{ps}$ | 5 |
| $L$ | 340 $\mu$H | $f_s$ | 5 kHz |
| $L_r$ | 140 $\mu$F | $C_r$ | 7.2 $\mu$F |
| $C_{l,p}$, $C_{l,s}$ | 1.0 mF | $L_h$ | 1.3 $\mu$H |
| $C_{h,p}$, $C_{h,s}$ | 1.0 mF | $L_l$ | 50 $\mu$H |
| $V_f$ | 20 V | $R_{r,avg}$ | 0.1 Ω |

Secondly, according to the ZVC characteristics, reactive current limits of PS-DAB and capability of overloading, the rated value of $d$ and the leakage inductance $L$ can be determined. In this case, $d$=0.2, and $L$=340$\mu$H.

Thirdly, the total number is finite, which makes it possible to test all the combinations of $N_p$ and $N_s$. In the rated voltage condition, $N_v$ should be ensured within a reasonable range, and in the meanwhile, $N_s$ should be as larger as possible. In the case, all of the combinations satisfy the limits.

At last, the worst condition needs to be checked according to (38) to ensure the secure operation of PS-DAB. If there is no suitable combination of $N_p$ and $N_s$, we may say that the requirements of the application are too harsh for HMDCSST. In this case, $N_p$=1 and $N_s$=4, which makes PS-DAB work beyond the voltage limit. So in this case, $N_p$=2 and $N_s$=3 is the best combination.

Figure 17 (a) shows that all the combinations of $N_p$ and $N_s$ satisfy the ZVS limit under the rated voltage, but the combination of $N_p$=1 and $N_s$=4 makes $N_v$ ($M$) out of the range of $M_{min}$ and $M_{max}$, as shown in Fig. 17 (b) and (c). Other combinations satisfy the limits of (38) though HMDCSST lose ZVS at the light load, in which the combination with the largest $N_s$ is the best choice. If the limits of operating voltage range change, the most suitable combination of $N_p$ and $N_s$ changes too, so there is no universal optimal ratio of $N_p$/$N_s$ valid for variable situations.

## V. Simulation and Experiment Verification

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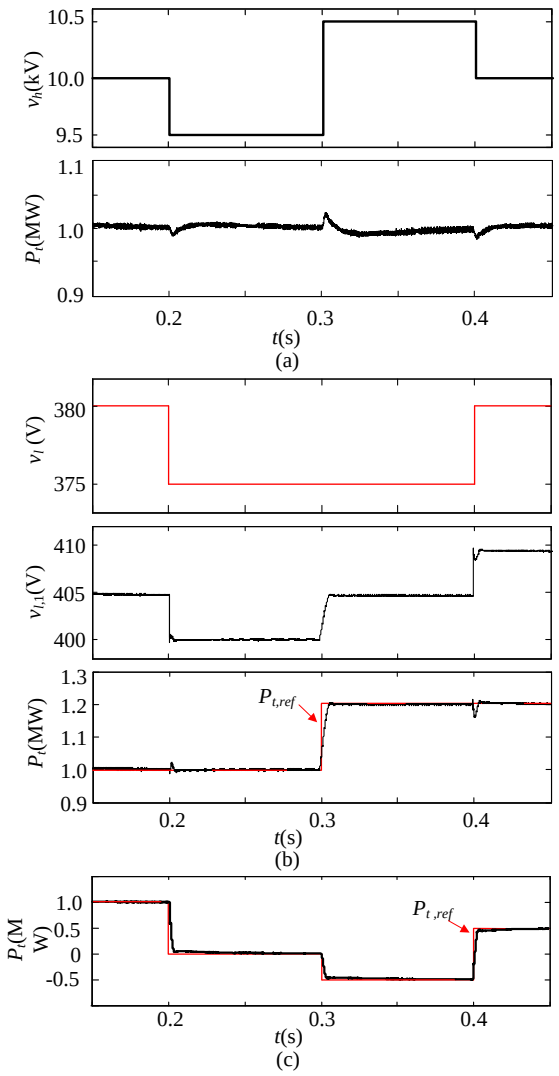


Fig. 18. Simulation waveforms in constant power control mode, under (a) MVDC bus disturbance; (b) LVDC bus disturbance and power reference step change; (c) power reference step change

### *A. Simulation Verification*

The validity of the proposed modeling method has been proved by MATLAB/Simulink in subsection E of Section II. In this Section, the performance of the proposed controller design is tested by MATLAB/Simulink based on the parameters summarized in Table I as well. For convenience, $v_h$ and $v_l$ are regarded as ideal voltage sources in the above theoretical analysis shown in Fig. 7. In the simulation, the resistance $R_h$ and $R_l$ between the grid bus and the HMDCSST in the high voltage and low voltage side should be considered.

Three cases are carried out to test the performance of the controller design. First, when the constant power control mode is applied to HMDCSST, the waveforms under various disturbances are drawn and plotted in Fig. 18. The initial steady-state operating voltage of MVDC bus is 10kV, then the voltage step changes to 9.5kV, 10.5kV, and 10kV at 0.2s, 0.3s, 0.4s respectively. The corresponding power response is illustrated at the bottom of Fig. 18(a). In Fig. 18(b), the LVDC bus voltage $v_l$ changes between 380V and 375V at 0.2s and 0.3s respectively, while the power reference $P_{t,ref}$ steps from 1.0MW to 1.2MW at 0.3s at the same time. The corresponding responses of output voltage $v_{l,1}$ and the transmitted power $P_t$ are given. In Fig. 18(c), the transmitted power following multi step changes of its reference. The results shown in Fig. 18 verified the effectiveness of HMDCSST in constant power control mode.

Similarly, the responses of HMDCSST to various disturbances under the constant voltage control are given in Fig. 19. As can be seen, against both input and output voltage disturbances, the output voltage can be controlled to track the given value of 400V.

Finally, to test the inrush current attenuation effect of the limiter 2, responses to a step change of the power reference (constant power control) without and with limiter 2 are shown in Fig. 20. When the limiter is absent in Fig. 20(a), the transient peak current of the PS-DAB, $i_L$, reaches -600A (about 12 times than the current at steady state), and the transient peak current of the SR-DAB resonant tank, $i_r$, reaches 200A (1.5 times than steady state). In comparison, when limiter 2 is added in Fig. 20(b), both the transient peak of the tank currents, $i_L$ and $i_r$, are reduced (in this case, the transient peak of $i_L$ is about 100A, and the transient peak of $i_r$ is about 80A). Furthermore, due to the attenuation of the transient peak current, the settling time of the transmitted power has been shortened from 30ms to 6ms approximately. It can be seen that limiting the average virtual current $i_l^*$ through a limiter can not only reduce the current inrush, but also enable the system to enter the steady state faster.

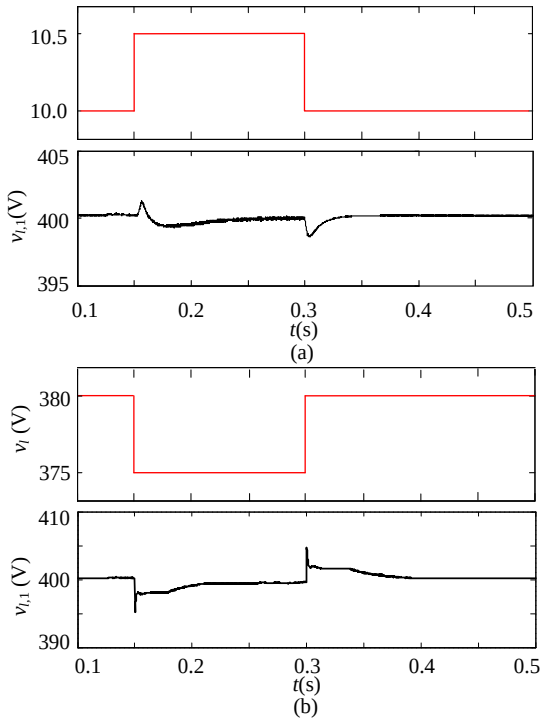


Fig. 19. Simulation waveforms in constant voltage scenario, (a) MVDC bus disturbance; (b) LVDC bus disturbance.

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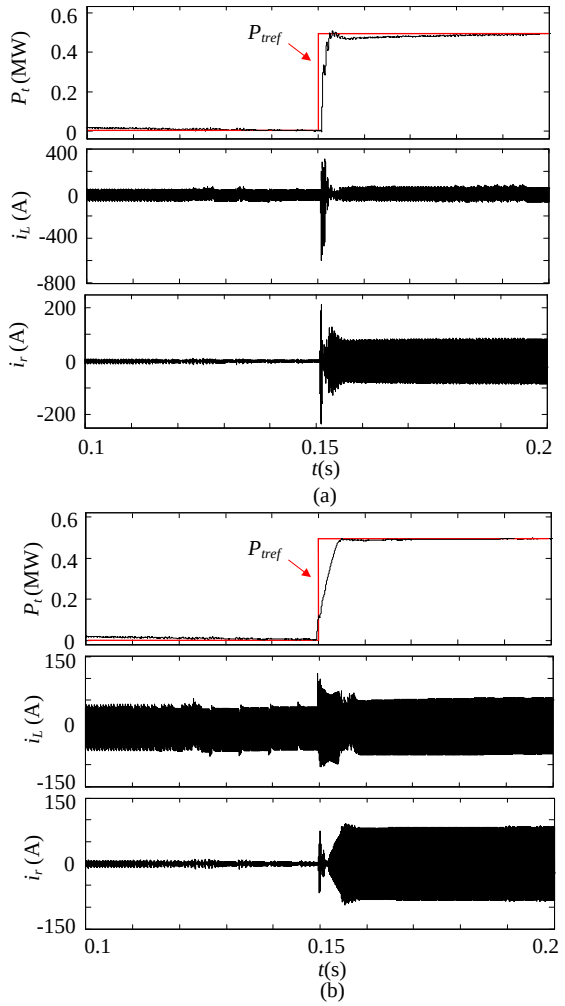


Fig. 20. Step response waveforms of power transmission, (a) without limiter 2; (b) with limiter 2.

### *B. Experiment Results*

To better verify the improving effect of the proposed HMDCSST in efficiency, a simplified experimental prototype consisting of one PS-DAB module and two SR-DAB modules was developed, as shown in Fig. 21. In the system configuration (Fig. 21(a)), a three-phase uncontrolled rectifier bridge is used to maintain the high voltage dc bus at 220V by adjusting the ac voltage regulator manually. To simulate the low dc grid, a battery stack is connected to the low-voltage dc bus through a DC-DC converter to maintain the low-voltage dc bus $v_l$' at 72V. And in case of bidirectional power flow verification, a resistor $R_h$' is connected in parallel on the high-voltage side to provide a branch for reverse power flow. $R_l$' is the resistance between the HMDCSST and the low-voltage dc grid.

Figure 21(b) is the picture of the prototype. In the main control unit (MCU) and in each PS-DAB module, a DSP chip of TMS320F28335 is put for the validation of the proposed control algorithm, and a Xilinx XC3S400 FPGA chip is responsible for processing the communication tasks and/or generating the firing pulses. Specifically, the MCU DSP receives the voltage sampling data from the FPGA, and generates the phase shift signals through the control program, and then sends them to the PS-DAB module. The SR-DAB modules operate under 50% duty cycle open loop control, and do not need communication optical fiber. Table II gives the experimental parameters. For fair comparison, the conventional DCSST uses three PS-DABs with single phase shift control. The rated power is 500 W, the same as that of the PS-DAB in the HMDCSST.

First, experimental curves of the transfer efficiency of HMDCSST are shown in Fig. 22(a) in the bidirectional power range. Corresponding results of the conventional DCSST based on PS-DAB purely are also given for comparison. As can be observed, the power transmission efficiency of the proposed HMDCSST is always higher than that of the pure PS-DAB based DCSST in the entire output power range. And the two efficiency curves have similar trend. The maximum efficiency of the HMDCSST is about 94.2% at about 400W, a significant improvement compared with the conventional one which is about 91.7%. The efficiency is about 10% higher compared with the conventional DCSST in light load condition (about 100W).

The loss analysis is performed as shown in Fig. 22 (b) and Fig. 22 (c). The loss breaking down of PS-DAB and SR-DAB at different load is displayed in Fig. 22(c), in which the loss of SR-DAB is always less than that of PS-DAB as expected. The switching loss of SR-DAB is nearly zero thanks for its ZCS. The conduction loss and transformer loss of SR-DAB are also less than those of PS-DAB, for the so-called circulated current exists in the PS-DAB with single phase shift control. Under light load, PS-DAB's switching loss is high for the lack of ZVS. So, it is clear that the SR-DABs contribute to the HMDCSST's efficiency improvement.

The measured input voltage unbalance factor $N_v$ is displayed in Fig. 23 of which the trend is consistent with theoretical analysis.

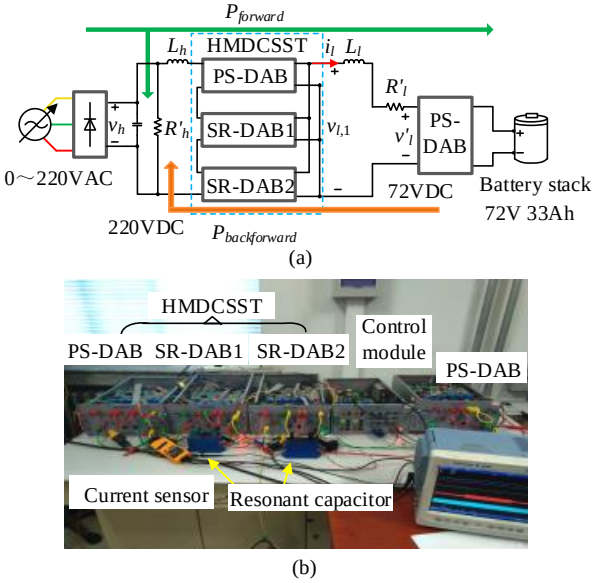


Fig. 21. Experimental system of HMDCSST, (a) System configuration, (b) Picture of the laboratory setup.

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TABLE II
EXPERIMENT PARAMETERS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_h$ | 220 V | $L_r$ | 141 $\mu$H |
| $V_l$ | 72 V | $L$ | 240 $\mu$H |
| $N_{ps}$ | 3 | $f_s$ | 5 kHz |
| $n_p$, $n_s$ | 1 | $C_{h,p}$, $C_{h,s}$ | 2.4 mF |
| $C_{l,p}$, $C_{l,s}$ | 2.4 mF | $C_r$ | 7.25 $\mu$F |
| $L_h$ | 7.4 $\mu$H | $L_l$ | 7.4 $\mu$H |
| $R_l$' | 1 Ω | $R_h$' | 96 Ω |

Secondly, detailed waveforms of the two types of DAB modules of HMDCSST in bidirectional power flow (100W and -100W) operation are provided in Fig. 24. Figure 24(a) and (b) show the waveforms of the PS-DAB in bidirectional power flow respectively, including the ac square-wave voltages of the primary/secondary side H bridges, $v_{h,p}$ and $v_{l,p}$, and the current of the HFT, $i_L$. Figure 24(c) and (d) show the square-wave voltages of the SR-DAB module in bidirectional power flow, $v_{h,s}$ and $v_{l,s}$, and the resonant current, $i_r$ respectively. It can be seen that the PS-DAB works in hard switching mode when the system operates under light load (100W/-100W), whereas the SR-DAB always works in ZVS/ZCS mode irrespective of the load condition, which is one of the reasons why the proposed HMDCSST can increase the efficiency in contrast with the conventional one based on PS-DAB purely.

The experimental step change responses of the power reference and the high/low voltage dc buses under constant power control are depicted in Fig. 25. As can be seen in Fig. 25(a), the output current can follow the reference value quickly. In Fig. 25(b), the high voltage dc bus $v_h$ changes from 220V to 210V, and then steps back to 220V after 4.5s; in Fig. 25(c), the low-voltage dc bus $v_l$' changes from 71V to 73V, and then goes back to 71V after 4.5s. In both cases, the HMDCSST can regulate its transmitted power.

Figure 26 shows the experimental responses under constant voltage control under various disturbances. In Fig. 26(a), the output voltage $v_{l,1}$ quickly track its reference value which changes from 72V to 71V and goes up to 73V. In Fig. 26(b), the voltage of the high voltage dc bus $v_h$ changes from 220V to 210V and goes back to 220V after 3.8s. In Fig. 26(c), the voltage of the low-voltage dc bus $v_l$' changes from 73V to 71V and goes up to 73V after 4.0s. In both cases very small voltage deviations are observed under the high and low voltage dc bus disturbances. In addition, the tank currents including the inductance current of the PS-DAB, $i_L$, and resonant current of the SR-DAB, $i_r$, are all provided in Fig. 25 and Fig. 26.

## VI. DISCUSSION

In this paper, both the PS-DAB and the SR-DAB employ the simplest topology and control strategy to illustrate the concept of HMDCSST. In fact, there are some issues need to be considered further.

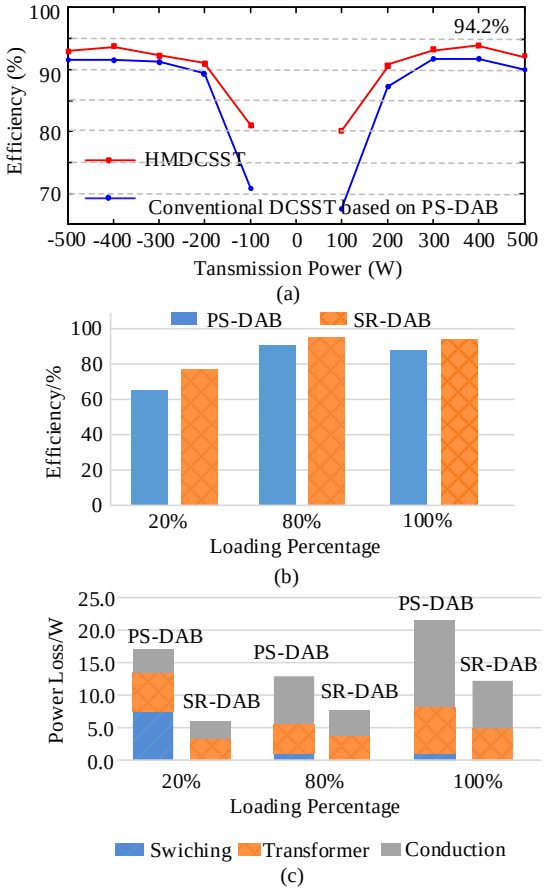


Fig. 22. Experimental measured efficiency and loss breaking down (a)Comparison between the proposed HMDCSST and the conventional DCSST based on PS-DAB purely;(b) Measured efficiency of PS-DAB and SR-DAB;(c) Power loss breaking down of PS-DAB and SR-DAB.

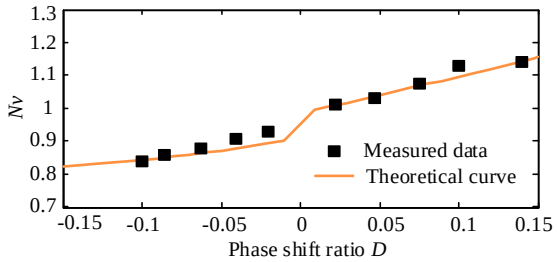


Fig. 23. Measured and theoretical input voltage unbalance ratio between SR-DAB and PS-DAB.

For PS-DABs, some control methods which have obvious advantages, such as triple phase-shifting control as mentioned in Section I, can be used to improve the ZVS and reactive current characteristics of PS-DAB, which is good for improving the efficiency and widening the voltage operation range of HMDCSST. Besides, the current sharing among PS-DABs can be improved by utilizing auxiliary voltage-balancing control [34].

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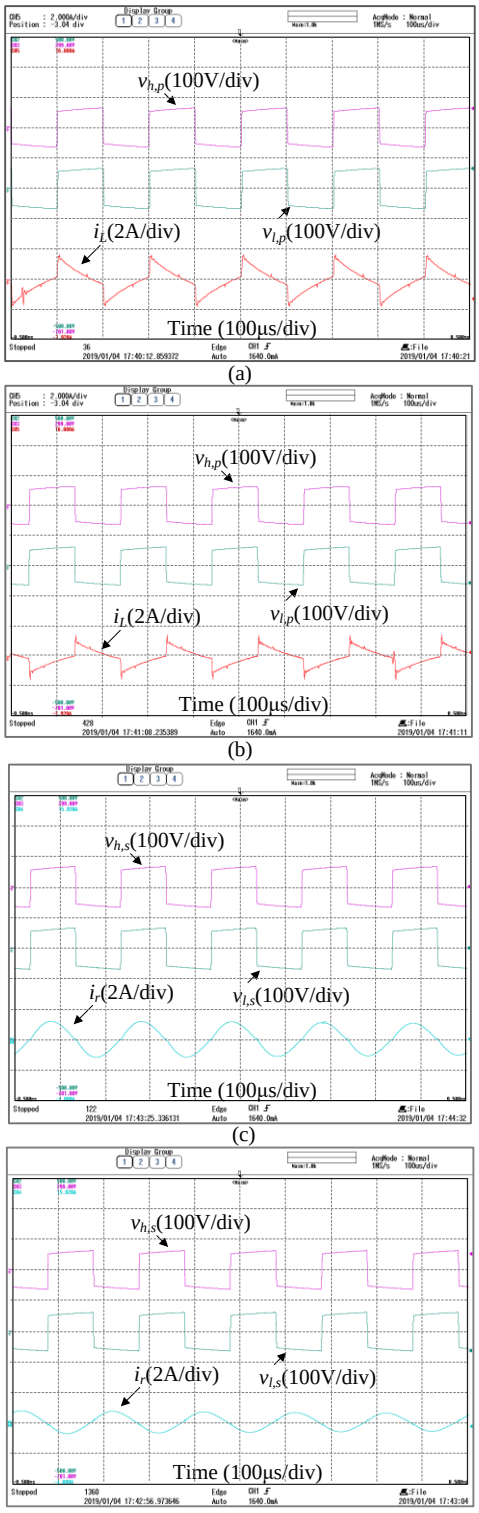


Fig. 24. Sub-module voltage/current waveforms in bidirectional power conditions (a) waveforms of PS-DAB in forward power flow, (b) waveforms of PS-DAB in reverse power flow, (c) waveforms of SR-DAB in forward power flow, (d) waveforms of SR-DAB in reverse power flow

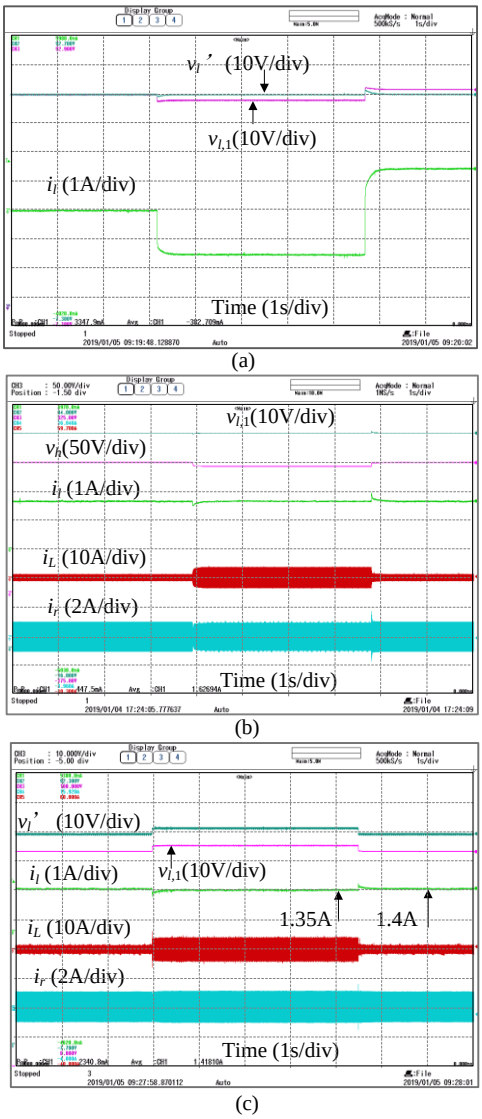


Fig. 25. Experimental responses under constant power control, under (a) power reference steps change; (b) high-voltage dc bus disturbance and (c) low-voltage bus disturbance.

For SR-DABs, there are some alternative topologies to improve the bidirectional performance, such as CLLC resonant converter. But in the HMDCSST, the SR-DABs work under completely resonance, thus the performance improvement needs to be investigated further. Since SR-DABs are uncontrolled in the HMDCSST, the current sharing among them may need some auxiliary circuits, such as a voltage balance converter [35].

The LC filters that affect the system dynamic performance have been discussed in Section II. In practical, the inductor also can be utilized as a limiter of the grid fault current, which can significantly suppress the peak values of the resonant current and the fault current of HMDCSST. Even so, the preventive measures such as overcurrent protection for the short circuit are still required.

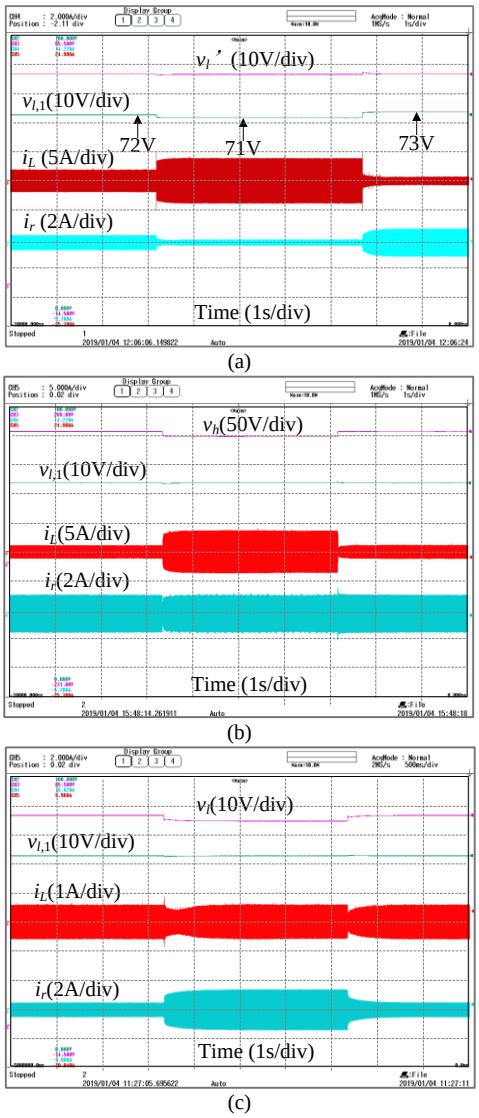


Fig. 26. Experimental responses under constant voltage control, under (a) output voltage reference steps change; (b) high-voltage dc bus disturbance and (c) low-voltage bus disturbance.

Since the HMDCSST is a general structure more than a certain topology, its performance could be optimized and improved in future. The original motivation for proposing the HMDCSST is to simplify the design and control of DCSST, reduce the components, processors and sensors, and ensure the system flexibility, reliability and efficiency. Therefore, the optimization objectives should be considered comprehensively and cover efficiency, reliability and cost and so on.

## VII. Conclusion

In order to improve the power transmission efficiency of the DC solid-state transformer and maintain a certain regulation capability of power and output voltage in the meanwhile, this paper proposes a hybrid modular DC solid-state transformer topology. The average model and low-frequency small-signal model of the new DCSST are firstly established, and the effect of the input/output LC filters on the system response characteristics is analyzed. Then two control strategies under the constant power and the constant voltage control are designed, and furthermore, the stability is analyzed. In particular, some designing problems with respect to the module number combinations of the two-type DABs in the HMDCSST are selected and discussed with both the characteristics of ZVS and the input voltage unbalance factor taken into consideration. Finally, simulation and experiments are performed to confirm the feasibility of the presented HMDCSST, which is characterized by better efficiency and simpler control compared with conventional DCSST based on PS-DAB purely, and the power/output voltage can be regulated with good performance.

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